Amendments to the Specification. Please amend the specification as follows:

Title:

Method, System And Program Product For A Pipelined Processor Having A Branch Target Buffer (BTB) To Create A Recent Entry Queue In Parallel With The Branch Target Buffer (BTB) ~~Effective Delayed, Minimized Switching, BTB Write Via Recent Entry Queue That Has The Ability To Delay Decode~~

Paragraph [0016]:

[0016] According to the method, system, and program product described herein, by keeping track of closely associated duplicates to become entries, the monitoring structure is extended to not only block BTB writes but to additionally notify instruction decode when such an operation is to take place. In the case of the majority of duplicate entries, the occurrence is initiated by an instruction loop where the first branch was not predicted in time because of branch prediction start-up latency which thereby causes each additional iteration to not be predicted in time. By being able to predict one ~~interaction~~ iteration of the loop, the BTB is able to get ahead and therefore potentially predict all future iterations of the branch point. By causing a delay in the pipeline by blocking the decoding operation, the branch prediction logic is able to get ahead thereby allowing the pipeline to run at the efficiency it is capable of. Such operations are viewable by higher performance which can be viewed externally as an application completing a task in a shorter time span.

Paragraph 19:

[0019] The method of operating a computer, the program product for operating a computer, and the computer having a pipelined processor with a branch target buffer (BTB) achieves these ends by creating a recent entry queue in parallel with the branch target buffer (BTB). The recent entry queue comprises a set of branch ~~transfer~~ target buffer (BTB) entries, which are organized as a FIFO queue, and preferable a FIFO queue that is full associative for reading.